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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 10/684,890	**Applicant(s)** JK KANG, JUN	
	Examiner Mai-Huong Tran	**Art Unit** 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-22 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,639,271 to Zheng et al. in view of the remark.

Regarding to claim 1, Zheng discloses a dielectric memory cell comprising a substrate 15 comprising a source region 19, a drain region 23, and a channel region 17 positioned there between; a multilevel charge trapping dielectric 12, 14, 16 positioned on the surface of the substrate 15; and a control gate 18 positioned on the surface of the multilevel charge trapping dielectric and positioned over and aligned with the channel region 17; and wherein the multilevel charge trapping dielectric includes a tunneling dielectric layer 12 adjacent to the substrate 15 comprising a first dielectric material of a tunnel dielectric layer thickness; a top dielectric layer 16 adjacent to the control gate 18 comprising a second dielectric material of a top dielectric thickness which is less than the tunnel dielectric thickness; a charge trapping layer 14 positioned between the tunneling dielectric layer 12 and the top dielectric layer 16. However, Zheng does not disclose wherein the control gate has a control gate conduction band Fermi level and a control gate valance band Fermi level; and wherein the difference between the control gate conduction band Fermi Level and a conduction band Fermi level of the top dielectric layer is less than the difference between the control gate valance band Fermi level and a valance band Fermi level of the top dielectric layer (col. 1, lines 48-60, and fig. 1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the control gate has a control gate conduction band Fermi level and a control gate valance band Fermi level; and wherein the difference between the control gate conduction band Fermi Level and a conduction band Fermi level of the top dielectric layer is less than the difference between the control gate valance band Fermi level and a valance band Fermi level of the top dielectric layer.

Regarding to claim 2, the dielectric memory cell wherein the control gate comprises polysilicon heavily implanted with a group III element (col. 1, line 53).

Regarding to claims 3, 4, 10, 11, 17, and 18, the dielectric memory cell wherein the first and second dielectric materials comprise silicon dioxide (col. 1, lines 15-24).

Regarding to claims 5, 12 and 19, the dielectric memory cell wherein the charge trapping layer comprises a nitride compound (col. 1, lines 1-24).

Regarding to claims 6, 13, and 20, the dielectric memory cell wherein the charge trapping layer is a nitride compound selected from the group of nitride compounds consisting of Si_2N_4, Si_3N_4, and SiO_xN_4 (col. 3, lines1-4).

Regarding to claims 7, 14, and 21, the dielectric memory cell wherein the second dielectric material is a dielectric selected from the group of an aluminum oxide compound, a Hafnium oxide compound, and a zirconium oxide compound (col. 5, lines 9-18).

Regarding to claims 8, 15, and 22, the dielectric memory cell wherein the second dielectric material is a dielectric selected from the group of Al_2O_3, $HfSi_xO_y$, HfO_2, ZrO_2, and $ZrXi_xO_y$ (col. 5, lines 9-13).

Regarding to claim 9, the dielectric memory cell wherein the control gate comprises a material selected from a group of materials consisting of GaN, ZnS, and C; and wherein such material is heavily implanted with a group III element (col. 1, line 53).

Regarding to claim 16, Zheng et al. discloses a charge trapping dielectric providing a non volatile storage of electrons in a dielectric memory cell, the charge trapping dielectric comprising a tunneling dielectric layer 28 adjacent to a substrate comprising a first dielectric material of a tunnel dielectric thickness; a top dielectric layer 36 adjacent to a control gate 38 comprising a second dielectric material having a top dielectric thickness, the top dielectric thickness being less than the tunnel dielectric thickness; and a charge trapping layer 34 positioned between the tunneling dielectric layer and the top dielectric layer (col. 4, lines 35-48, and fig. 2).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mai-Huong Tran